WHAT IS CLAIMED IS:

1. A non-volatile memory cell comprising:

a control gate pattern disposed over a semiconductor substrate and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern and a control gate electrode, which are stacked;

a selection gate electrode disposed over the semiconductor substrate at one side of the control gate pattern;

a gate insulation pattern interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern;

a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the semiconductor substrate under the selection gate electrode.

2. The non-volatile memory cell according to claim 1, wherein the tunnel insulation pattern is formed of at least one selected from the group consisting of silicon oxide and silicon oxynitride.

3. The non-volatile memory cell according to claim 1, wherein the trap insulation pattern is formed of at least one selected from the group consisting of silicon nitride, polysilicon dots and nitride dots.

4. The non-volatile memory cell according to claim 1, wherein the selection gate electrode is spacer-shaped and elongated to cover one sidewall and a top surface of the control gate pattern.

5. The non-volatile memory cell according to claim 1, wherein the thickness of the gate insulation pattern is less than the sum of the thickness of the tunnel insulation pattern, the trap insulation pattern and the blocking insulation pattern.

6. The non-volatile memory cell according to claim 1, further comprising drain/source regions formed in the semiconductor substrate at respective sides of the cell channel region, the drain region being in contact with the first channel region and the source region being in contact with the second channel region.

7. The non-volatile memory cell according to claim 1, further comprising a metal silicide layer formed over a predetermined region of a sidewall of the selection gate electrode, an exposed sidewall of the control gate electrode and a surface of the drain/source regions.

8. A non-volatile memory cell comprising:

a first control gate pattern and a second control gate pattern disposed in parallel over a semiconductor substrate, each of the first and second control gate patterns comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern and a control gate electrode, which are stacked sequentially;

a first selection gate electrode disposed, in parallel to the first control gate pattern, over the semiconductor substrate at one side of the first control gate pattern;

a second selection gate electrode disposed, in parallel to the second control gate pattern, over the semiconductor substrate at one side of the second control gate pattern;

a first gate insulation pattern interposed between the first selection gate electrode and the semiconductor substrate, and between the first selection gate electrode and the first control gate pattern;

a second gate insulation pattern interposed between the second selection gate electrode and the semiconductor substrate, and between the second selection gate electrode and the second control gate pattern;

a first cell channel region comprising a first channel region defined in the semiconductor substrate under the first control gate pattern and a second channel region defined in the semiconductor substrate under the first selection gate electrode; and

a second cell channel region comprising a first channel region defined in the semiconductor substrate under the second control gate pattern and a second channel region defined in the semiconductor substrate under the second selection gate electrode,

wherein the first and second selection gate electrodes are disposed symmetrically over the substrate.

9. The non-volatile memory cell according to claim 8, wherein the tunnel insulation patterns are formed of at least one selected from the group consisting of silicon oxide and silicon oxynitride.

10. The non-volatile memory cell according to claim 8, wherein the trap insulation patterns are formed of at least one selected from the group consisting of silicon nitride, polysilicon dots, and nitride dots.

11. The non-volatile memory cell according to claim 8, wherein the first selection gate electrode is spacer-shaped and elongated to cover one sidewall and a top surface of the first control gate

electrode and one sidewall of the first selection gate electrode, and the second selection gate electrode is spacer-shaped and elongated to cover one sidewall and a top surface of the second control gate electrode.

12. The non-volatile memory cell according to claim 8, wherein the selection gate electrodes are disposed between the control gate patterns.

13. The non-volatile memory cell according to claim 12, further comprising:

a first drain region in contact with the first channel region of the first cell channel region;

a second drain region in contact with the first channel region of the second cell channel region; and

a source region in contact with the second channel region of the first cell channel region and the second channel region of the second cell channel region .

14. The non-volatile memory cell according to claim 8; wherein the control gate patterns are disposed between the selection gate electrodes.

15. The non-volatile memory cell according to claim 14, further comprising:

a first source region in contact with the second channel region of the first cell channel region;

a second source region in contact with the second channel region of the second cell channel region; and

a drain region in contact with the first channel region of the first cell channel region and the first channel region of the second cell channel region.

16. The non-volatile memory cell according to claim 9, wherein the thickness of each gate insulation pattern is less than the total thickness of the tunnel insulation pattern, the trap insulation pattern and the blocking insulation pattern.

17. A method of fabricating a non-volatile memory cell comprising the steps of:

forming a tunnel insulation layer, a trap insulation layer, a blocking insulation layer, a first gate conductive layer and a hard mask layer sequentially on a semiconductor substrate;

forming a stepped groove exposing a predetermined region of the semiconductor substrate by patterning the hard mask layer, the first gate conductive layer, the blocking insulation layer, the trap insulation layer,

and the tunnel insulation layer successively, wherein the tunnel insulation layer, the trap insulation layer, the blocking insulation layer and the first gate conductive layer form protruding portions of the stepped groove;

forming a spacer-shaped selection gate electrode covering protruding portions of the stepped groove and a gate insulation pattern, which is interposed between the selection gate electrode and an inner sidewall of the stepped groove, and between the selection gate electrode and the semiconductor substrate;

forming a control gate pattern having a sidewall that is self-aligned with a sidewall of the gate insulation pattern, wherein the control gate pattern comprises the tunnel insulation layer, the trap insulation layer, the blocking insulation pattern and the control gate electrode which are stacked sequentially.

18. The method of fabricating a non-volatile memory cell according to claim 17, wherein the tunnel insulation layer is formed of at least one selected from the group consisting of silicon oxide and silicon oxynitride.

19. The method of fabricating a non-volatile memory cell according to claim 17, wherein the trap insulation layer is formed of at least one selected from the group consisting of silicon nitride, polysilicon dots and nitride dots.

20. The method of fabricating a non-volatile memory cell according to claim 17, wherein the step of forming the stepped groove comprises the steps of:

forming a first groove, which exposes a predetermined region of the first gate conductive layer by patterning the hard mask layer;

forming spacers which have an etch selectivity with respect to the first gate conductive layer on sidewalls of the first groove;

forming a second groove, using the hard mask layer and the spacers as an etching mask, exposing a predetermined region of the semiconductor substrate by aniostropic etching successively the blocking insulation layer, the trap insulation layer and the tunnel insulation layer; and

removing the spacers, wherein the stepped groove comprises the first and second grooves.

21. The method of fabricating a non-volatile memory cell according to claim 17, wherein the step of forming a selection gate electrode and a gate insulation pattern comprises the steps of:

forming a gate insulation layer over the entire semiconductor substrate including the stepped groove;

forming a second gate conductive layer over the gate insulation layer; and

aniostropically etching successively the second gate conductive layer and the gate insulation layer.

22. The method of fabricating a non-volatile memory cell according to claim 17, wherein the step of forming a control gate pattern comprises the steps of:

forming a protection layer over an exposed surface of the semiconductor substrate and on a curved sidewall of the selection gate electrode; and

anisotropically etching the hard mask layer, the first gate conductive layer, the blocking insulation layer, the trap insulation layer and the tunnel insulation layer using the protection layer and the gate insulation pattern as an etch mask, wherein the protection layer is formed of a material layer having an etch selectivity with respect to the hard mask layer and the first gate conductive layer, and

wherein the control gate pattern is equivalent to the protruding portion of the stepped groove.

23. The method of fabricating a non-volatile memory cell according to claim 22, wherein the protection layer is formed of thermal oxide.

24. The method of fabricating a non-volatile memory cell according to claim 17, further comprising a step of forming impurity diffusion layers by selectively implanting impurity ions in the semiconductor substrate at sides of the selection gate electrode.

25. The method of fabricating a non-volatile memory cell according to claim 24, further comprising a step of forming a metal silicide layer on predetermined regions of the impurity diffusion layers, predetermined regions of a sidewall of the selection gate electrode and the self-aligned sidewall of the control gate electrode.

26. A method of fabricating a non-volatile memory cell comprising the steps of:

forming a tunnel insulation layer, a trap insulation layer, a blocking insulation layer, a first gate conductive layer and a hard mask layer sequentially over a semiconductor substrate;

forming a line pattern composed of a preliminary tunnel insulation pattern, a preliminary trap insulation pattern, a preliminary blocking insulation pattern, a first gate electrode pattern and a hard mask pattern

which are stacked by successively patterning the hard mask layer, the first conductive layer, the blocking insulation layer, the trap insulation layer and the tunnel insulation layer, wherein the first gate conductive pattern, the preliminary blocking insulation pattern, the preliminary trap insulation pattern and the preliminary tunnel insulation pattern form protruding portions of the line pattern;

forming a spacer-shaped selection gate electrode covering the protruding portion of the line pattern, and a gate insulation pattern interposed between the selection gate electrode and the line pattern, and between the selection gate electrode and the semiconductor substrate; and

forming a control gate pattern having a sidewall self-aligned with the gate insulation pattern, wherein the control gate pattern comprises a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern and a control gate pattern, which are stacked.

27. The method of fabricating a non-volatile memory cell according to claim 26, wherein the tunnel insulation layer is formed of at least one selected form the group consisting of silicon oxide, silicon oxynitride.

28. The method of fabricating a non-volatile memory cell according to claim 26, wherein the trap insulation layer is formed of at least one selected from the group consisting of silicon nitride, polysilicon dots and nitride dots.

29. The method of fabricating a non-volatile memory cell according to claim 26, wherein the step of forming a line pattern comprises the steps of:

forming the hard mask pattern line-shaped by patterning the hard mask layer on the first gate conductive layer;

forming spacers having an etch selectivity with respect to the first conductive layer on sidewalls of the hard mask pattern;

forming a preliminary tunnel insulation pattern, a preliminary trap insulation pattern, a preliminary blocking insulation pattern and a first gate conductive pattern by anisotropically etching the first gate conductive layer, the blocking insulation layer, the trap insulation layer and the tunnel insulation layer using the hard mask and the spacers as an etch mask;

removing the spacers, wherein the line pattern comprises the preliminary tunnel insulation pattern, the preliminary trap insulation pattern, the preliminary blocking insulation pattern, the first conductive layer and the hard mask pattern.

30. The method of fabricating a non-volatile memory cell according to claim 26, wherein the step of forming a selection gate electrode and a gate insulation pattern comprises the steps of:

forming a gate insulation layer conformally on the entire semiconductor substrate including the line pattern;

forming a second gate conductive layer on the gate insulation layer;

anisotropically etching the second conductive layer and the gate insulation.

31. The method of fabricating a non-volatile memory cell according to claim 26, wherein the step of forming the control gate pattern comprising the steps of:

forming a protection layer over an exposed surface of the semiconductor substrate and on a curved sidewall of the selection gate electrode;

ansiotropically etching the hard mask pattern, the first gate conductive pattern, the preliminary blocking insulation pattern, the preliminary trap insulation pattern and the preliminary tunnel insulation pattern using the protection layer and the gate insulation pattern as an etch mask, wherein the protection layer is formed of a material layer

having etching selectivity with respect to the hard mask layer and the first gate conductive layer, and wherein the control gate pattern is equivalent to the protruding portion of the line pattern.

32. The method of fabricating a non-volatile memory cell according to claim 31, wherein the protection layer is formed of thermal oxide.

33. The method of fabricating a non-volatile memory cell according to claim 26, further comprising a step of forming impurity diffusion layers by selectively implanting impurity ions in the semiconductor substrate at sides of the selection gate electrode.

34. The method of fabricating a non-volatile memory cell according to claim 33, further comprising a step of forming a metal silicide layer on a predetermined region of the impurity diffusion layer, a predetermined region of a sidewall of the selection gate electrode and the self-aligned sidewall of the control gate electrode.